REMARKS

The Office Action of January 26, 2007, has been received and reviewed.

Claims 1, 3, 5-25, 28-35, 53, and 54 are currently pending in the above-referenced application. Each of claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 has been considered and stands rejected.

Claims 9, 24, and 29 have been withdrawn from consideration.

Claim 3 has been canceled without prejudice or disclaimer.

Reconsideration of the above-referenced application is respectfully requested.

Utility Rejections under 35 U.S.C. § 101

Claims 1, 3, 5-8, 10-17, and 53 stand rejected under 35 U.S.C. § 101 because the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility.

A claimed invention must have a specific, substantial, and well-established utility. M.P.E.P. § 2107. A "specific utility" is *specific* to the subject matter claimed and can provide a well-defined and particular benefit to the public. M.P.E.P. § 2107.01(I). A "substantial utility" defines a "real world" use. *Id.*

Applicant respectfully submits that claims 1, 3, 5-8, 10-17, and 53 meet the utility requirement because the specification discloses a practical or real world benefit for the resiliently compressible spacers.

In the Office Action, it is asserted that "the claim limitation, 'resiliently compressible' is not supported by either a specific and substantial asserted utility or a well established utility." Office Action, page 3. However, it is respectfully submitted that a "resiliently compressible spacer" has specific and substantial utility, non-limiting examples of which are provided in the as-filed specification. Specifically, paragraph [0013] discloses that "[n]onlinear spacers may be shaped in such a manner as to impart them with some resilient compressibility upon receiving a force in the directions of the lengths thereof." *See* Specification, paragraph [0013]. Furthermore, FIGs. 10A-10D of the as-filed specification depict how the resiliently compressible spacers (40a-

40d) may be used to facilitate semiconductor device assembly. *Id.*, paragraph [0047]; FIGs. 10A-10D.

Because the resiliently compressible spacers have at least one specific and substantial utility, withdrawal of the 35 U.S.C. § 101 rejections of claims 1, 3, 5-8, 10-17, and 53 is respectfully requested, as is allowance of each of these claims.

35 U.S.C. § 112 Claim Rejections

Claims 1, 3, 5-8, 10-17 and 53 stand rejected under 35 U.S.C. § 112, first paragraph, because one of ordinary skill in the art purportedly would not know how to use the claimed spacers. This is apparently a rejection under the enablement requirement of the first paragraph of 35 U.S.C. § 112.

It is respectfully submitted that one of ordinary skill in the pertinent art would readily understand, from the disclosure of the as-filed specification, the context in which the resiliently compressible spacers are used and how to use the resiliently compressible spacers in a semiconductor device assembly. FIGs. 10A-10D of the as-filed specification specifically show non-limiting examples of how resiliently compressible spacers (40a-40d) may be used in a semiconductor device assembly. *Id.*, paragraph [0047]; FIGs. 10A-10D. As another non-limiting example, the as-filed specification describes how resiliently compressible spacers may be used to receive force in a semiconductor assembly. *Id.*, paragraph [0013].

Therefore, it is respectfully submitted that each of claims 1, 3, 5-8, 10-17, and 53 complies with the enablement requirement of 35 U.S.C. § 112, first paragraph. As such, withdrawal of the 35 U.S.C. § 112, first paragraph, rejections of claims 1, 3, 5-8, 10-17, and 53 is respectfully solicited, as is allowance of each of these claims.

Objections to Claims

Claim 25 has been objected to for being of improper dependent form for failing to further limit the subject matter of a previous claim. In particular, it has been asserted that claim 25 fails to further limit the subject matter from the claim from which it depends.

It is respectfully submitted that claim 25 recites an additional structural element and, thus, is a proper dependent claim. Specifically, claim 25, which depends from claim 23, recites that the mutually laterally spaced discrete spacers of dependent claim 23 are in communication with a ground or reference voltage plane of the first semiconductor device. As claim 23 does not includes such a requirement, it is respectfully submitted that claim 25 further limits the subject matter recited in claim 23.

As such, it is respectfully submitted that claim 25 further limits the subject matter recited in another claim, as required by 37 C.F.R. § 1.75(c).

Rejections under 35 U.S.C. § 103(a)

Claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 have been rejected under 35 U.S.C. § 103(a). The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Hikita in View of Eldridge

Claims 1, 3, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53, and 54 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent 6,724,084 to Hikita et al. (hereinafter "Hikita") and U.S. Patent 6,835,898 to Eldridge et al. (hereinafter "Eldridge").

Hikita teaches a semiconductor device with two IC chips that are electrically connected with active surfaces in opposition. The IC chips are electrically connected by functional bumps BF1 and BF2 connected to an internal circuit and surrounding the active regions on the IC chips.

Col. 11, lines 44-50. Dummy bumps BD1 and BD2 are provided in opposed relation, isolated from the internal circuits on the front faces 11 and 21 of the IC chips. Col. 11, lines 50-56. The dummy bumps BD1 and BD2 are positioned to support the central portion of the IC chips. Col. 12, lines 20-26.

Eldridge teaches resilient electrical contacts that may be used to interconnect terminals of electrical components. Col. 58, lines 41-43. The resilient contacts originate from terminals on a first electrical component and terminate at terminals on another electrical component. Col. 57, lines 45-67. Thus, Eldridge describes resilient contacts bound to a terminal or bond pad on opposing active surfaces of semiconductor dice.

Independent claim 1, as amended and presented herein, is drawn to a semiconductor device assembly that includes at least one semiconductor device and at least one resiliently compressible spacer protruding from an active surface of the at least one semiconductor device. The at least one resiliently compressible spacer defines a distance that the active surface of the at least one semiconductor device is to be spaced apart from the back side of another semiconductor device, which is to be positioned in superimposed relation with the at least one semiconductor device.

It is respectfully submitted that there are at least two reasons that a *prima facie* case of obviousness has not been established against any of claims 1-5, 7-19, 34, 36-45, or 47.

First, neither Hikita nor Eldridge teaches or suggests a spacer that defines a distance that the active surface of at least one semiconductor device is to be spaced apart from the back side of another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device. Rather, both Hikita and Eldridge teach structures positioned between opposing active surfaces of semiconductor dice. More specifically, Hikita teaches dummy bumps BD1 and BD2 that are respectively positioned on a "front face" 11 and 21 of the primary chip 1 and the secondary chip 2. Hikita teaches that the front face "is a surface of the semiconductor substrate...on the side of an active surface region." *See* Hikita, col. 11, lines 33-36. Referring to FIG. 5 of Hikita, the dummy bumps BD1 and BD2 are positioned between opposing active surfaces (e.g., front faces 11 and 21) of the primary chip 1 and secondary chip 2. *Id.*, FIG. 5. Because Hikita is limited to a stacked device with active surfaces

of a primary chip 1 and secondary chip 2 facing each other, Hikita does not teach semiconductor devices positioned in superimposed relation.

Eldridge teaches contact structures that electrically connect electronic components. More specifically, the one end of the contact structure is fabricated on a terminal of one electronic component and the other end of the contact structure is bonded a terminal on another, oppositely facing electronic component. Because the description of Eldridge is limited to contact structures used to connect electronic components with active surface facing one another, Eldridge does not teach or suggest electronic components positioned in superimposed relation to one another.

Second, it is respectfully asserted one of ordinary skill in the art would not have been motivated to combine the teachings of Hikita and Eldridge in the manner that has been asserted. Specifically, one of skill in the art would not be motivated to combine the teachings of Hikita relating to dummy bumps BD1 and BD2 that protect the chips from stress caused by resin sealing with the teachings of Eldridge relating to electrical contacts. Hikita explicitly states that "the dumpy bump BD1 and the dummy bump BD2 do not serve for the electrical connection between the primary chip 1 and secondary chip 2." *See* Hikita, col. 12, lines 30-32. Moreover, the dummy bumps BD1 and BD2 of Hikita are positioned to support the central portions of the stacked IC chips. In contrast, the contact structures of Eldridge are configured to provide electrical connections between semiconductor devices, but no not provide support for one semiconductor device positioned over another semiconductor device.

Thus, it is respectfully submitted that a *prima facie* case of obviousness has not been established against claim 1, as is required to maintain a rejection under 35 U.S.C. § 103(a). Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of claim 1 is respectfully requested.

Claims 3, 5-8, 10-17 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 1, which is allowable.

Independent claim 18 is drawn to a semiconductor device assembly that includes a substrate, a first semiconductor device associated with the substrate, bond pads of the first semiconductor device in communication with corresponding contact areas of the substrate, a mutually laterally spaced discrete spacers positioned on and protruding from an active surface of

the first semiconductor device, at least one spacer of the mutually laterally discrete spacers in communication with a ground or reference voltage plane of the first semiconductor device and a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane.

Neither Hikita nor Eldridge teaches or suggests a second semiconductor device comprising a back side positioned on mutually laterally spaced discrete spacers. Rather, both Hikita and Eldridge teach semiconductor devices configured with active surfaces facing each other as described with respect to claim 1. Moreover, one of skill in the art would not be motivated to combine the teachings of Hikita relating to non-conductive dummy bumps configured to support stacked IC chips with the teachings of Eldridge relating to contact structures that facilitate electrical connection between electronic devices.

It has been asserted that "the term 'back' is a relative term, and the side of the second semiconductor facing the active surface of the first semiconductor device is inherently at least the back side relative to the side opposite the back." Office Action, page 7. However, as evidenced by Hikata, it is known to those of ordinary skill in the art that an "active surface" of a semiconductor device is a surface upon which integrated circuitry has been fabricated. Thus, it is respectfully submitted that, relative to the "active surface" of the semiconductor device, the "back side" of the semiconductor device refers an opposite surface. The Office Action refers to McFarland to show that "the scope of the term 'back side' is not limited to the non-active side of a semiconductor device." *Id.* According to the Office, McFarland defines "the terms 'frontside,' 'backside,' and 'sides' of a die" to "refer to the sides of a semiconductor chip or a die which carries integrated circuitry." *See* McFarland, paragraph [0018]. Notably, it is the die of McFarland that carriers integrated circuitry, not all of the "sides" of the die. Thus, it is respectfully submitted that a more appropriate reading of paragraph [0018] of McFarland is that a semiconductor chip or die that carries integrated circuitry includes a "frontside," a "backside," and "sides."

Furthermore, McFarland makes it clear that the definitions for the terms "frontside," "backside," and "sides," as used therein, only apply to the four corners of that document. *See, id.*

Moreover, McFarland does not refer to an "active surface" of a semiconductor device. *See* McFarland, paragraph [0018]. Thus, it is respectfully submitted that the terms "active surface" and "back side" should not be interpreted contrary to common usage based on McFarland.

Thus, it is respectfully submitted that a *prima facie* case of obviousness has not been established against claim 18, as is required to maintain a rejection under 35 U.S.C. § 103(a). Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of claim 18 is respectfully requested.

Each of claims 19-23, 25, 28, 31, 32, 34, 35, 53, and 54 is allowable, among other reasons, for depending directly or indirectly from independent claim 18, which is allowable.

Hikita in View of Eldridge and Pu

Claims 16, 30, and 33 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over that taught in Hikita and Eldridge as applied to claims 15 and 18, and further in combination with U.S. Patent 6,593,662 to Pu et al. (hereinafter "Pu").

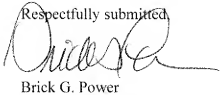
Each of claims 16, 30, and 33 is allowable, among other reasons, for depending either directly or indirectly from independent claim 18, which is allowable.

Withdrawal of the 35 U.S.C. § 103(a) rejections of claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 is respectfully requested, as is the allowance of each of these claims.

CONCLUSION

It is respectfully submitted that each of claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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